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Energy-Efficient Phase-Change Memory with Graphene as a Thermal Barrier

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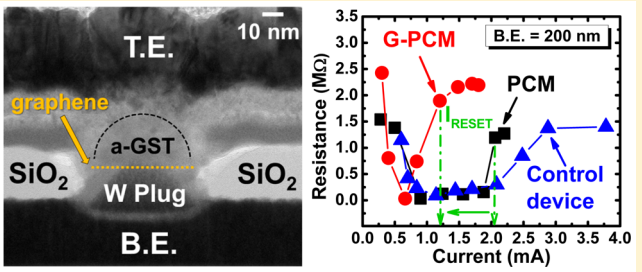
Supporting Information

ABSTRACT: Phase-change memory (PCM) is an important class of data storage, yet lowering the programming current of individual devices is known to be a significant challenge. Here we improve the energy-efficiency of PCM by placing a graphene layer at the interface between the phase-change material, $Ge_2Sb_2Te_5$ (GST), and the bottom electrode (W) heater. Graphene-PCM (G-PCM) devices have ~40% lower RESET current compared to control devices without the graphene. This is attributed to the graphene as an added interfacial thermal resistance which helps confine the generated heat inside the active PCM volume. The G-PCM achieves programming up to 10^5 cycles, and the graphene could further enhance the PCM endurance by limiting atomic migration or material segregation at the bottom electrode interface.



KEYWORDS: *Graphene, Joule heating, phase-change memory, reset current, thermal boundary resistance*

Phase-change memory (PCM)[1−5] has been one of the leading candidates of emerging nonvolatile memories, mainly due to its great scalability down to the single-digit nanometer regime.[6−11] PCM has superior performance compared to mainstream NAND Flash, with cycling endurance up to 10^9 demonstrated[12,13] and faster switching speed of less than 10 ns.[14] The phenomenon of resistive switching in PCM is based on the reversible phase transition of chalcogenide alloys between low-resistance crystalline and high-resistance amorphous phases,[1] caused by current-induced Joule heating. Because crystallization (for SET) and melting (for RESET) of the phase-change material occurs at relatively high temperatures (around 150 °C[15] for crystallization to the fcc-phase $Ge_2Sb_2Te_5$ (GST) and over 600 °C[16] for GST melting), relatively high programming (RESET) currents remain a challenge for PCM. Although reduction of I_{RESET} down to the μA range has been demonstrated using individual carbon nanotube electrodes,[7,8,10,11] a more scalable approach to energy-efficient PCM is needed.

For a given technology node, the strategy for reducing the programming current of PCM falls into two complementary categories: materials engineering and thermal engineering. Examples of materials engineering include the use of GeTe/Sb_2Te_3 superlattices for interfacial[17] and charge-injection[18] PCMs, as well as the use of nanocrystalline doped GST.[19] Thermal engineering aims to achieve PCM heating with minimal current by increasing the thermal resistance and thermal confinement of PCM. The early invention of the confined PCM cell structure[20] was a prototypical approach of thermal engineering, and the use of thermally confined TaN/TiN bottom electrode (BE) in the conventional mushroom structure[21,22] has also been effective. For the PCM to be more energy-efficient, the Joule heating should be restricted inside a small volume of the phase-change material and heat loss by thermal conduction to the surroundings needs to be minimized. One approach to achieve this has been to engineer the interface between the phase-change material and the metal heater.[23−25] For example, PCM with a semiconducting fullerene film (~30 nm C_{60}) inserted at the interface between GST and metal bottom electrode[24] has shown up to ~70% reduction of I_{RESET}. However, such interfacial films with a relatively large thickness (~10 nm for TiO_2,[23] about 30 nm for C_{60},[24] and over 100 nm for WO_3[25]) may not be an ideal solution because they introduce series resistance[24] and may degrade the PCM reliability.[23]

In this work, we demonstrate the use of graphene as an *atomically thin* interfacial thermal barrier between the PCM and the heater electrode. Although graphene has a large in-plane thermal conductivity,[26] the out-of-plane heat flow across monolayer and few-layer graphenes is strongly limited by its weak van der Waals interfaces.[27−29] In fact, the cross-plane thermal resistance of graphene is estimated to be equivalent to that of ~25 nm of SiO_2 but with subnanometer thickness,[26] depending

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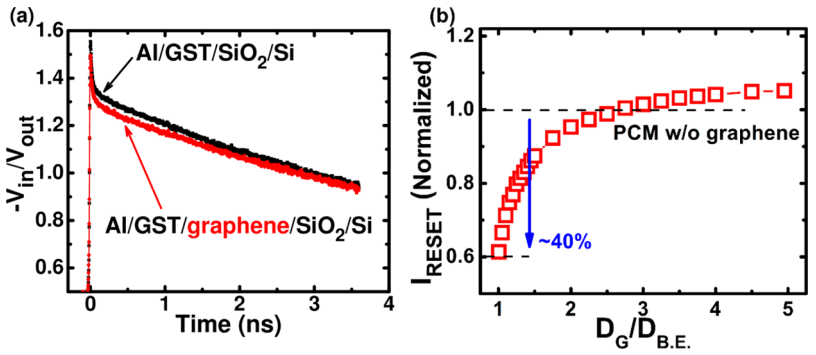

Figure 1. (a) TDTR (time-domain thermoreflectance) measurements of the ratio of the in-phase (V_{in}) and out-of-phase (V_{out}) components of the reflected probe intensity, comparing the film stacks (see Figure S1) with and without the graphene. The inserted graphene layer leads to a slower thermal decay, thus indicating that it adds a significant amount of thermal resistance in the out-of-plane direction. (b) Simulated RESET programming current of the G-PCM as a function of ratio between the graphene width and the bottom electrode width (D_G/D_{BE}). I_{RESET} is normalized to that of the conventional PCM. Also see Figure S2.

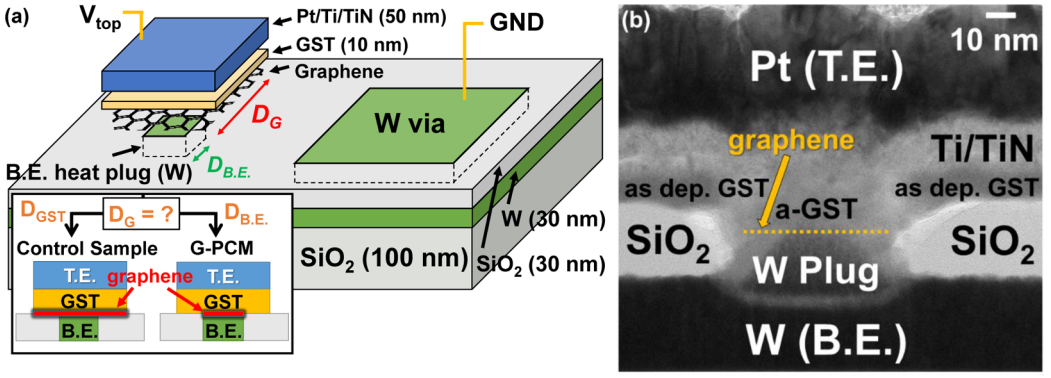

Figure 2. (a) Schematic representation of the G-PCM device fabricated in this work. The top electrode voltage (V_{top}) is applied to the Pt/Ti top electrode, and the larger area W via, which connects the smaller e-beam patterned heat plug through the bottom electrode underneath, is electrically grounded. Two different types of PCM devices are fabricated with different graphene sizes (D_G) as a comparison (inset). D_G is set at 1 μm, equal to D_{GST} for the control sample, while D_G varies with the effective contact diameter ($D_G = D_{BE}$) for the G-PCM. (b) Cross-sectional HR-TEM image of the G-PCM device in the high-resistance state (HRS) with typical resistances of a few MΩ's and the effective contact size (the diameter of the columnar W heater plug) ~ 100 nm. The TEM cannot resolve the subnanometer thick graphene; thus, its location is shown by an arrow at the a-GST (amorphous GST) interface with the W-plug. See Figure S5; some physical damage to the graphene is observed after the 10 nm GST film is sputtered on top.

on the adjacent materials.[30] Consequently, we insert a graphene layer at the interface between GST and metal (W) bottom electrode to confine heating of the PCM and form a novel graphene-PCM (G-PCM) device structure. The interfacial graphene layer is patterned by electron-beam lithography (EBL) to be as small as the effective contact area of the PCM. About 40% reduction in RESET current of the fabricated G-PCM structure is achieved with minimal increase in electrical contact resistance of the graphene, and high programming endurance is also maintained. This study demonstrates a practical electronic application of graphene as a thermal barrier for heat-sensitive devices and systems such as PCM.

In order to understand the thermal effect of the graphene layer, we first investigated the out-of-plane thermal resistance of Al (80 nm)/GST (10 nm)/graphene/SiO_2 (285 nm)/Si stacks by employing the time-domain thermoreflectance (TDTR) technique (see Figure 1a). TDTR is a well-established pump−probe technique, capable of measuring the cross-plane thermal conductivity of nanometer-thin films and thermal conductance per unit area across interfaces of particular interest[27] (see Supporting Information, Section 1 and Figure S1). Compared to control test structures without the graphene in the stack, the TDTR measurement with the graphene exhibited a slower thermal response (Figure 1a), corresponding to an increased thermal boundary resistance (TBR). The inserted graphene layer and its interfaces added a TBR of 32 ± 10 and 44 ± 3 m^2K/GW for graphene interfaces with as-deposited (amorphous) and annealed (fcc-crystalline phase) GST films, respectively, at room temperature. These values are remarkable, demonstrating how a subnanometer thin graphene can serve as an effective thermal barrier. This cross-plane TBR of the graphene is equivalent to the thermal resistance of a much thicker layer of 10−15 nm GST, while occupying negligible volume within an overall PCM bit.

Using the measured TBR values for the graphene and its interfaces, we also performed an electro-thermal COMSOL[31] analysis (see Figure 1b and Supporting Information Section 2) to assess how effective the graphene is as a thermal barrier in the practical PCM device structure. Temperature profiles were simulated for typical mushroom-type PCM structures, except that graphene of different sizes (of area D_G^2, where D_G is the dimension of the graphene) were inserted at the interface between the GST and the metal (W) heater. We compared the impact of different dimensions of the graphene interfacial layer in Figure 1b, in terms of the normalized RESET-programming current. Because the graphene has >100× higher in-plane

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thermal conductivity than out-of-plane,[26] its width affects the heating efficiency of the PCM cell. When the graphene covers a larger area, the efficiency in heating up the thin GST film (10 nm) becomes lower due to heat flow along the graphene lateral direction. It is therefore necessary to limit the inserted graphene layer in the PCM into a much smaller region than that of the GST layer on top. By doing so, one can more fully utilize the benefits of the graphene as a thermal barrier in the out-of-plane direction while minimizing the heat lost along the in-plane direction. The temperature profile in Figure S2 suggests that when the graphene is patterned as small as the W heater underneath ($D_G \approx 215$ nm), the hottest region inside the active GST volume can reach as high as its melting temperature (T_{melt} = 900 K in the simulation) with the lowest RESET current applied.

Based on the observations made in Figure 1a and b, we fabricated the novel G-PCM device structure (see Figure 2a and b), where the interfacial graphene thermal barrier enables an energy-efficient PCM design, as follows (see Figure S3 for the details of device fabrication). The 30 nm W layer is first electron-beam (e-beam) evaporated to serve as the bottom electrode, followed by 30 nm of SiO_2 by plasma-enhanced chemical vapor deposition (PECVD). The 100 kV EBL is then applied to pattern the nanoscale via, and the subsequent processes of dry-etching the dielectric layer and filling via holes with e-beam evaporated W are precisely calibrated such that the surface of the W plug is nearly flush with the oxide surface (<10 nm) after lift-off (see Figure S4 for the top view SEM image of the e-beam patterned vias). A graphene layer purchased from Graphene Supermarket[32] is then transferred using a typical poly (methyl methacrylate) (PMMA) scaffold[33] and patterned by EBL to be as small as the bottom W heater electrode, i.e., $D_G = D_{BE}$. The 10 nm GST is sputtered directly on top of the graphene layer (see Figure S5 for Raman data for graphene), followed by a TiN adhesion layer (10 nm), a Ti layer (10 nm), and Pt (30 nm) top electrode. As shown in the inset of Figure 2a, a control sample is separately prepared with the graphene patterned into a much larger area of $D_G = D_{GST}$ and compared with the optimal design of the G-PCM with $D_G = D_{BE}$.

The typical threshold switching behavior of the fabricated G-PCM devices is presented in Figure 3 for a DC current sweep. Here G-PCM devices with $D_G = D_{BE}$ = 100 nm are compared with control PCM devices without graphene that have various bottom electrode contact sizes (D_{BE}). For both G-PCM and PCM, the large conductivity increase occurs at the voltage above the threshold point ($V_T \sim 5.5$ V), accompanied by a well-known voltage snap-back. The threshold switching is the key electrical process which enables current-induced phase change to occur in PCM devices. The fabricated G-PCM device shows similar DC threshold switching as the control PCM device of the same size (100 nm) without the graphene. One difference is that device-to-device variation of the low-resistance state (LRS) resistance (R_{LRS}) after SET seems larger for the G-PCM device. R_{LRS} of the G-PCM device varies from about 50 to 200 kΩ for the effective contact size of 100 nm, while that of the control PCM device of the same size ranges from 40 to 50 kΩ. Since the LRS resistance of the PCM is the sum of the resistances of the heater element (columnar W-plug), the phase-change material (GST), and various interfaces, the difference in the distribution of R_{LRS} between the G-PCM and the PCM is attributed to the imperfect graphene interfaces. It is noteworthy that we successfully minimized the electrical contact resistance of graphene by (1) keeping the PMMA support layer fresh before graphene transfer and (2) optimizing the conditions for PMMA removal after graphene transfer, and for e-beam resist removal after graphene patterning. Additionally, other approaches may be implemented to further reduce contamination of the graphene surface.[34−37]

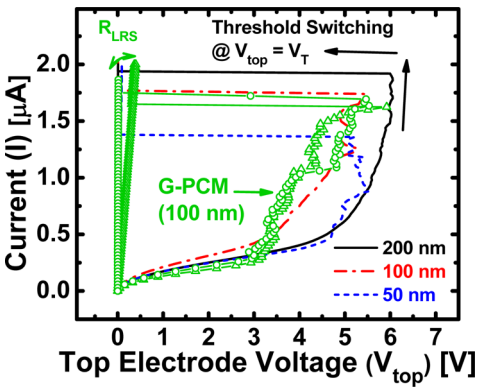

Figure 3. SET threshold switching characteristics of fabricated PCM devices with different BE sizes of 200, 100, and 50 nm, and G-PCM devices with $D_G = D_{BE}$ = 100 nm. Device-to-device variation in the low-resistance state (LRS) of G-PCM indicates that imperfect graphene interfaces (ostensibly arising from PMMA residues after graphene transfer and from the GST sputtering process) should be carefully treated to minimize the electrical contact resistance of graphene.

Next, in order to explore the potential advantage of the G-PCM in achieving lower RESET current (I_{RESET}), we compared the R-I (resistance vs current) switching characteristics of three different PCM devices fabricated in Figure 4: G-PCM with $D_G = D_{BE}$, PCM without the graphene, and control sample with D_G = 1 μm. We first consider the typical R-I behavior of the conventional PCM device without the graphene. Programming currents with small pulse amplitudes (<0.5 mA) lead to the

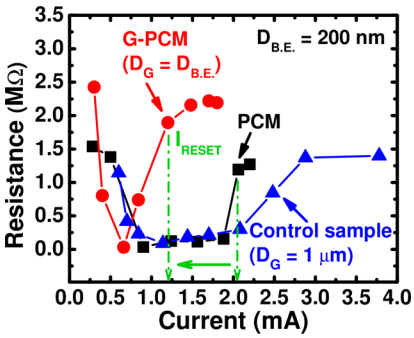

Figure 4. RESET current reduction in the G-PCM device (with patterned graphene), compared with control samples without the graphene and with a wider graphene layer (D_G = 1 μm). The switching curves were obtained by applying a 10 ns/100 ns/10 ns (rise time/duration/fall time) voltage pulse with increasing voltage amplitude to the PCM top electrode, and monitoring the waveform through the 50 Ω internal resistance of the oscilloscope. All three types of PCM devices considered had the same bottom electrode size (D_{BE} = 200 nm). About 40% decrease of I_{RESET} in the G-PCM compared to the PCM without graphene, points to the enhanced confinement of heat by the inserted graphene layer at the interface. The G-PCM device with the smallest contact resistances (i.e., the smallest R_{LRS}, comparable to that of the traditional PCM) was used in the pulsed switching experiment. The cycle-to-cycle distribution of I_{RESET} for the 200 nm G-PCM is shown in Figure S7.

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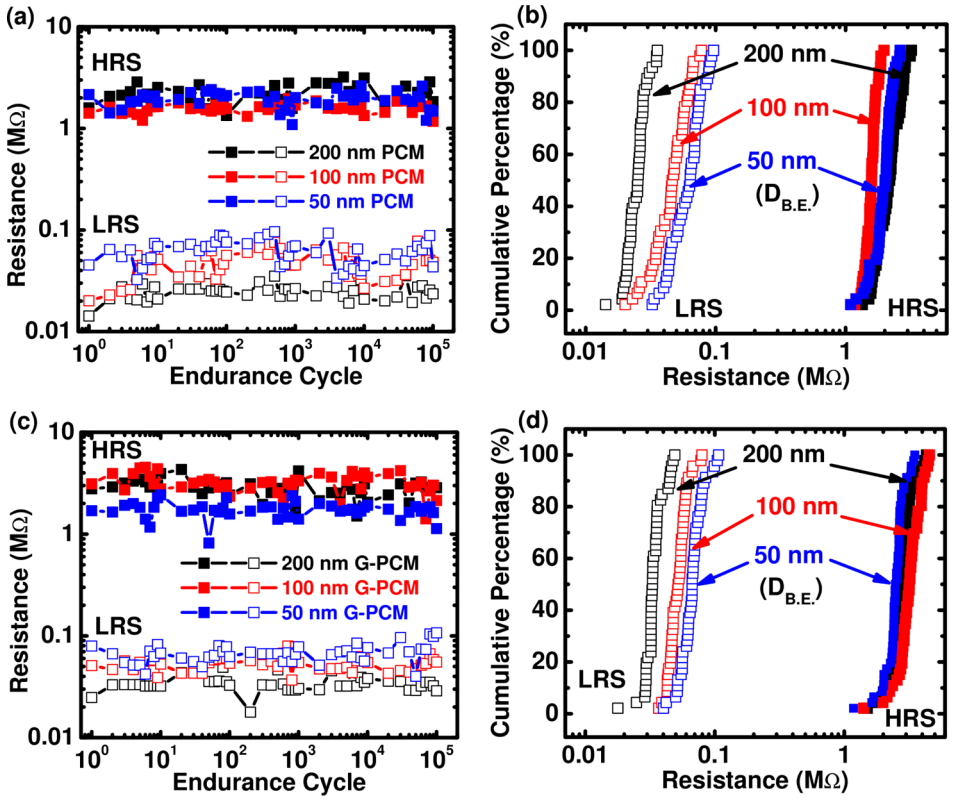

Figure 5. (a) Pulsed write/erase endurance characteristics and (b) cycle-to-cycle resistance distributions of the PCM control devices (without graphene) fabricated with varying BE sizes, D_{BE} = 200, 100, and 50 nm. (c and d) Similar plots for the G-PCM devices with patterned graphene, D_G = D_{BE}. For electrical switching, voltage pulses of 1 μs/100 μs/1 μs and 10 ns/50 ns/10 ns were applied for SET (write) and RESET (erase), respectively. Both types of devices can be switched up to 10^5 cycles, with an on/off resistance ratio between 30 and 100.

initial annealing of the active amorphous volume of the GST and the consequent decrease in the cell resistance. As the current increases and approaches the value of I_{RESET}, the melt-and-quench of the critical volume results in an increase of the cell resistance, and the RESET transition occurs. The measured I_{RESET} of about 2 mA for the 200 nm control PCM without graphene is in agreement with a trend line[1] of the linear relationship between the RESET current and the effective contact area of the PCM (see Supporting Information Figure S6 for the measured I_{RESET} values as a function of the PCM bottom electrode size, for both PCM and G-PCM). It is significant that the PCM devices fabricated in this study require relatively low programming current densities (J_{RESET}) of <7 MA/cm^2 (see the inset of Figure S6). Carefully designed PCM cell structures have been programmed typically at J_{RESET} ~ 10 MA/cm^2.[1]

Compared with the control PCM without graphene, the G-PCM exhibits 40% smaller RESET programming current, I_{RESET} ~ 1.2 mA, although it has the same effective contact diameter, D_{BE} ≈ 200 nm (see Figure S7 for the cycle-to-cycle distribution of measured I_{RESET}). As shown by our earlier measurements and simulations (Figure 1), this occurs because the interfacial graphene layer (patterned by EBL as small as the W heater plug) limits the generated heat from being dissipated through the plug into the bottom electrode of the PCM. The critical role of the inserted graphene layer as an effective thermal barrier is also supported by the fact that I_{RESET} of the control sample (with D_G = 1 μm, see Figure 2a) is similar to or a bit larger than that of the conventional PCM. If the observed I_{RESET} reduction in the G-PCM resulted in part from added series resistance of the graphene and its interfaces, the control sample would also have led to a smaller I_{RESET} than the traditional PCM, as it also had the interfacial layer of graphene. Since the larger graphene in this control sample conducts more heat in the in-plane direction than the EBL patterned graphene in the G-PCM, it heats a larger GST volume on top, canceling out the advantage in I_{RESET} reduction.

It should be noted that the G-PCM device used for the pulsed switching experiments in Figure 4 (and the one in Figure 5) had R_{LRS} comparable to that of the PCM device without graphene. This is important, as the minimal electrical contact resistance due to graphene can rule out the possibility of increased Joule heating, and confirms our reasoning of graphene-assisted heat confinement as the physical source of the reduced I_{RESET} in the G-PCM.

Another key challenge in utilizing low thermal conductivity thin films (thermal conductivity in the range of 0.4−1.7 W m^{-1} K^{-1} for TiO_2, C_{60}, and WO_3[23−25]) to engineer the interface between the phase-change material and the metal heater is the need to maintain the endurance of the integrated PCM device. Endurance characteristics have not been tested in many previous studies using interfacial thin films[24,25] or only a limited and degraded number of switching cycles have been reported.[23] The difficulty arises from the fact that the thin film inserted at the phase-change material interface with the metal heater could participate in physical interactions (atom intermixing or alloying) with the adjacent phase-change atoms, as the interface is very hot during programming. In this regard, Figure 5, which displays the endurance characteristics and the resistance distributions for both PCM (Figure 5a

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and b) and G-PCM (Figure 5c and d) devices, is of great importance in verifying a functional G-PCM device. First, the G-PCM device shows excellent electrical performance, as compared with earlier studies using other thin films.[23−25] We achieved good programming endurance of up to 10^5 cycles in the G-PCM, along with tight cycle-to-cycle resistance distributions and on/off resistance ratios of ∼30, ∼60, ∼100 for devices with $D_{BE} \approx$ 50, 100, and 200 nm, respectively. Second, it is interesting to note that the G-PCM did not exhibit any degradation in the memory window. The LRS resistance did not change even after the graphene insertion, owing to the minimal electrical contact resistance of graphene.

In general, the main cause to the endurance failure of PCM is the physical movement and segregation of phase-change atoms.[38,39] Graphene-inserted PCM may lead to higher endurance as compared to conventional structures because the graphene serves as a physical barrier[40,41] between the phase-change material and the metal heater, preventing atomic migration or material segregation that could occur at this interface during repeated programming cycles. However, in this work we did not observe improved endurance in devices with graphene at the interface; the endurance was limited to 10^5 cycles for both PCM and G-PCM devices for unidentified reasons which will be the focus of future work. Nevertheless, our study suggests that graphene is a good candidate for an interfacial material to improve the thermal efficiency of the PCM and possibly increases the endurance of the PCM as well. As an added advantage, the inserted graphene layer gives no degradation in electrical performance of the PCM while improving the thermal efficiency.

In summary, we have found that graphene is a uniquely suited material for interfacial thermal engineering of the PCM, as it is atomically thin and chemically inert due to strong sp^2 carbon bonds. We experimentally demonstrated that graphene-inserted PCM devices consume less programming current (using lower power), with the best results obtained when the graphene was patterned to the same width as the bottom electrode. These devices showed 40% lower RESET current compared with traditional PCM devices of the same effective contact size, while still maintaining fast switching speed of sub-50 ns (for RESET), high programming endurance of up to 10^5 cycles, and good on/off resistance ratio between 30 and 100. The reduced I_{RESET} is attributed to the thermal boundary resistance of graphene and its interfaces, leading to improved thermal efficiency of the device by restricting heating within the active programming region of the PCM.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.5b02661.

Details of the TDTR (time−domain thermoreflectance) measurements, 3D finite-element (COMSOL) simulation, process flow for fabricating the G-PCM (graphene-inserted PCM) device, SEM image of the electron-beam patterned W plug and via, Raman spectroscopy for graphene, measured RESET current (I_{RESET}) as a function of the effective contact diameter of the PCM/G-PCM, and cycle-to-cycle distributions of measured I_{RESET} for PCM and G-PCM devices (PDF)

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Notes

The authors declare no competing financial interest.

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